IN THE CLAIMS:

1. (Amended) A semiconductor wafer device comprising:

a semiconductor wafer having a circuit area disposed in a central area of said semiconductor wafer and a peripheral area of said semiconductor wafer not formed with circuits;

a number of semiconductor elements formed in the circuit area;

a multi-layer wiring structure formed in the circuit area and having multi-layer wirings connected to said semiconductor elements and interlevel insulating films, at least some of the multi-layer wirings being damascene wirings including wiring patterns and via conductors embedded in the interlevel insulating films; and

a multi-layer structure formed in the peripheral area, having insulating films made of a same materials as the interlevel insulating films and conductor patterns, defined between sidewalls of said insulating films, made of same materials as the wiring patterns and not having conductor patterns corresponding to the via conductors.

Please add new Claim 22, as follows

22. (New) The semiconductor wafer device according to claim 1, wherein:

said interlevel insulating films include a first insulating layer having a lower dielectric constant than silicon oxide and formed over said semiconductor wafer in an area excepting a peripheral area of said underlying structure, and a second insulating layer having a dielectric constant higher than said first insulating layer and formed on said first insulating layer and the device further comprises said second insulating layer or a layer of a same material as the conductor covering an

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outermost side wall of said first insulating layer.